REMARKS

The Final Office Action mailed on October 11, 2002, has been received and reviewed.

Claims 1 through 3, 5 through 41, and 43 through 55 are currently pending in the above-referenced application. Claims 4, 42 and 57 through 72 were canceled without prejudice or disclaimer in the Amendment dated July 8, 2002.

Each of claims 1 through 3, 5 through 41, and 43 through 55 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

Claims 1 through 3, 5 through 41, and 43 through 55 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,004,867 to Kim et al. (hereinafter "Kim") in view of U.S. Patent 5,990,546 to Igarashi et al. (hereinafter "Igarashi"), U.S. Patent 5,682,062 to Gaul (hereinafter "Gaul"), and U.S. Patent 5,229,647 to Gnadinger (hereinafter "Gnadinger").

It is respectfully submitted that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Kim teaches chip-scale packages and methods for forming such chip-scale packages. The chip-scale packages of Kim include a semiconductor device, or die, and a substrate which may comprise silicon and upon which terminals are located and by which electrical traces are carried. The terminals of the substrate are arranged correspondingly to the arrangement of bond pads on the semiconductor device. *See, e.g.,* FIG. 2. The substrate may include one or more layers of conductive traces. *See, e.g.,* FIG. 2; col. 3, lines 26-28; FIG. 3; col. 4, lines 47-51.

While Kim teaches that the conductive traces may be located anywhere *in* the substrate (col. 3, line 55), Kim does not teach or suggest that the conductive traces may be carried upon a

surface of the substrate which is to be located opposite a semiconductor device with which the substrate is to be assembled. To the contrary, the terminals and conductive traces are fabricated on an active surface of a semiconductor substrate, which ultimately becomes the bottom surface of the resulting substrate, by known semiconductor device fabrication processes. Col. 4, lines 13-18. Since conventional semiconductor device fabrication processes are used, material of the semiconductor substrate must be removed from the backside thereof, which ultimately becomes the top of the resulting substrate, so that terminals or other electrically conductive features may be exposed at both surfaces of the wafer. *See* FIG. 5D; col. 6, lines 19-21. Consequently, the only conductive features that are carried upon the surface of the substrate that is to be located opposite a semiconductor device are the terminals.

Igarishi teaches a much different type of substrate that may be used in a chip-scale package. The substrate of Igarishi is a tape-automated bonding (TAB) type structure in which a routing conductor (*i.e.,* conductive traces) is sandwiched between two insulating layers. Col. 4, lines 38-45; FIGs. 1(A)-8. The teachings of Igarishi are limited to the use of a "metallic foil[-]laminated synthetic resin film" to form the substrate. Col. 5, lines 21-23. The substrate may be formed Terminals, or "electrodes", extend through both of the insulating layers to facilitate rerouting of the bond pads of a semiconductor device positioned adjacent to one side of the substrate to alternate locations on the opposite side of the substrate to provide the resulting chip-scale package with a desired connection pattern. Col. 4, lines 38-45; FIGs. 1(A)-8. Igarishi does not teach or suggest that conductive traces may be carried on a surface of the substrate. Rather, the teachings of Igarishi are limited to substrates with internally-extending conductive traces.

Gaul teaches semiconductor wafers which have conductive vias positioned between adjacent dice formed thereon. The vias extend from the active surfaces of the wafers to the backsides thereof. The conductive vias facilitate stacking the wafers and semiconductor dice and electrical connection of the stacked wafers or semiconductor devices to one another. Alternatively, the backsides of the semiconductor devices of Gaul may be positioned against substrates and the semiconductor devices electrically connected to the substrates by way of receptacles formed in or contact pads formed on the backsides of the semiconductor devices. *See*

FIG. 4-G; col. 8, line 65, to col. 9, line 16; FIG. 6; col. 11, lines 20-41. The conductive traces that are taught in Gaul extend laterally from the conductive vias along the active surface of the wafer. When another, similar wafer is stacked on top of the wafer described in Gaul, these conductive traces are positioned adjacent the backside of the overlying wafer. *See, e.g.*, FIG. 4P.

Another package described in Gaul includes a thick overcoat of dielectric material formed over the active surface of a semiconductor device. The overcoat does not carry contacts, conductive traces, or any other conductive structures.

Gaul does not teach or suggest a substrate. Moreover, Gaul lacks any teaching or suggestion that any of the conductive structures described therein, which are located between adjacent semiconductor devices, may be positioned adjacent to the active surface of a separate semiconductor device. Instead, the teachings of Gaul are limited to assemblies that include conductive vias in alignment with one another.

Gnadinger teaches a semiconductor device with through holes that extend partially through the thickness thereof. The through holes extend from conductively doped regions of silicon (diffusion regions 23) that are located beneath contact pads (*e.g.*, bond pads) on the active surface of the semiconductor device to the backside of the semiconductor device. Accordingly, when the semiconductor device is positioned over another, solder ball bearing semiconductor device with a through hole over a solder ball, during reflow of the solder, the solder may extend up into the through hole and contact a diffusion region 23, which communicates electrically with the overlying contact pad. In this manner, electrical connection may be established between or by way of the two adjacent semiconductor devices.

Independent claim 1, as proposed to be amended, recites a chip-scale package which includes a semiconductor device and a substrate disposed adjacent an active surface of the semiconductor device. The substrate comprises a semiconductor material. At least one electrically conductive via extends at least partially through the substrate, is positioned over the semiconductor device, and communicates with a corresponding bond pad of the semiconductor device. In addition, at least one conductive trace, which is in communication with the at least

one conductive via, is carried on a surface of the substrate which is opposite from the surface of the substrate that is adjacent to the semiconductor device.

It is respectfully submitted that a *prima facie* case of obviousness under 35 U.S.C § 103 of the pending claims of the above-referenced application cannot be established based merely on the teachings of Kim, Igarishi, Gaul, and Gnadinger.

First, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Kim, Igarishi, Gaul, and Gnadinger in the manner that has been asserted. Specifically, while Kim and Igarishi teach substrates that are configured for use in chip-scale packages, Gaul and Gnadinger teach multi-device wafers that are configured to be stacked with similar wafers such that bond pads of the semiconductor devices on different wafers may communicate with one another. Moreover, the substrates that are taught in Kim and Igarishi include conductive vias that are configured to be located over a semiconductor device of a chip-scale package, while the conductive vias of the wafers that are taught in Gaul and Gnadinger are not located over a semiconductor device but, rather, are positioned between adjacent semiconductor devices on their respective wafer.

In view of the diversity between the teachings of Kim and Igarishi and those of Gaul and Gnadinger, it appears that the only motivation to have combined the teachings of these references must have been based on improper hindsight provided by the teachings of the above-referenced application.

Second, it is respectfully submitted that one of ordinary skill in the art would have no reason to expect that the proposed combination of teachings from Kim, Igarishi, Gaul, and Gnadinger would successfully result in the subject matter recited in independent claim 1, as proposed to be amended, or in either independent claim 21 or independent claim 43. Again, while Kim and Igarishi teach substrates for chip-scale packages, which substrates include conductive vias that are configured to be positioned over a semiconductor device, Gaul and Gnadinger teach multi-device wafers that include conductive vias that are located between adjacent semiconductor devices and, rather than being configured to be positioned over a

semiconductor device, are configured to be aligned with contacts of a carrier substrate or corresponding conductive vias of another multi-device wafer.

Third, it is respectfully submitted that Kim, Igarishi, Gaul, and Gnadinger, taken either alone or in combination, do not teach or suggest each and every element of any of claims 1 through 3, 5 through 41, or 43 through 55.

In particular, with respect to independent claim 1, as proposed to be amended, none of Kim, Igarishi, Gaul, and Gnadinger teaches or suggests a chip-scale package which includes a semiconductor device and a substrate with at least one conductive trace that is in communication with at least one electrically conductive via positioned over the semiconductor device and that is carried on a surface of the substrate which is opposite from semiconductor device.

Rather, Kim teaches substrates that may include conductive traces on a bottom surface thereof (*i.e.*, a surface which contacts a semiconductor device when the substrate is assembled with the semiconductor device) or carried internally by the substrate.

The teachings of Igarishi are limited to substrates with internally confined conductive traces. *See, e.g.*, Igarishi, FIGs. 1(A)-8.

While the conductive traces of Gaul and Gnadinger may be carried by a surface of a multi-device bearing wafer which is located opposite another, underlying multi-device bearing wafer, these conductive traces do not communicate with a conductive via that is positioned over a semiconductor device. Instead, the conductive vias with which these traces communicate are located between adjacent semiconductor devices.

It is, therefore, respectfully submitted that, under 35 U.S.C. § 103(a), independent claim 1, as proposed to be amended, is allowable over Kim, Igarishi, Gaul, and Gnadinger.

Claims 2, 3, and 5 through 20 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Independent claim 21 also recites a chip-scale package that includes a substrate and a semiconductor device. The substrate of amended independent claim 21 comprises semiconductor material and includes a first surface with contact areas that are arranged correspondingly to an arrangement of bond pads on the semiconductor device, as well as

conductive vias extending therethrough and a second surface carrying at least one conductive trace that extends laterally from a conductive via. Amended independent claim 21 also recites that bond pads of the semiconductor device communicate through corresponding conductive vias of the substrate.

None of Kim, Igarishi, Gaul, or Gnadinger, taken either individually or together, teaches or suggests a chip-scale package which includes a semiconductor device and a substrate that includes a surface located opposite from the semiconductor device and that carries at least one conductive trace that extends laterally from a conductive via that communicates with a contact area positioned correspondingly to a bond pad of the semiconductor device. Rather, the conductive traces of Kim and Igarishi are located internally or on the same surface of the substrate as that against which a semiconductor device is positioned. Further, the conductive traces of Gaul and Gnadinger do not communicate with contact areas that are positioned correspondingly to bond pads but with conductive vias that are positioned between adjacent semiconductor devices.

It is, therefore, respectfully submitted that the combination of Kim, Igarishi, Gaul, and Gnadinger does not teach or suggest each and every element of independent claim 21.

Therefore, it is respectfully submitted that, under 35 U.S.C. § 103(a), independent claim 21 is allowable over Kim, Igarishi, Gaul, and Gnadinger.

Each of claims 22 through 42 is allowable, among other reasons, as depending either directly or indirectly from claim 21, which is allowable.

Independent claim 43 recites a flip-chip carrier. The flip-chip carrier of independent claim 43 includes a substrate that comprises semiconductor material. The substrate includes at least one via formed therethrough. A first end of the via is located proximate a first surface of the substrate and is positioned to substantially align with a corresponding bond pad of a semiconductor device to be assembled with the substrate. The substrate also includes at least one conductive trace laterally extending from a second end of the at least one via and carried by a second surface of the substrate.

Again, Kim, Igarishi, Gaul, and Gnadinger each lack any teaching or suggestion of a substrate with a first end of at least one via being positioned proximate a first surface so as to substantially align with a corresponding bond pad of a semiconductor device and at least one conductive trace carried by a second surface of the substrate and extending laterally from a second end of the via. As none of Kim, Igarishi, Gaul, or Gnadinger, taken either alone or in combination, teaches or suggests each and every element of independent claim 43, it is respectfully submitted that, under 35 U.S.C. § 103(a), independent claim 43 is allowable over each of these references.

Claims 44 through 55 are each allowable, among other reasons, as depending either directly or indirectly from claim 43, which is allowable.

For these reasons, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1 through 3, 5 through 41, and 43 through 55 be withdrawn.

ENTRY OF AMENDMENTS

It is respectfully submitted that this Amendment should be entered since the proposed changes to claim 1 and the remarks presented herein are supported by the as-filed specification and drawings, do not add any new matter to the application, and do not raise new issues or require a further search. If it is determined that this Amendment does not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

It is respectfully submitted that each of claims 1 through 3, 5 through 41, and 43 through 55 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,

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BGP/jml

Enclosure: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as follows:

1. (Twice Amended) A chip-scale package, comprising:

a semiconductor device including an active surface; and

a substrate comprising a semiconductor material disposed adjacent said active surface and including:

at least one electrically conductive via extending at least partially therethrough, positioned over said semiconductor device, and [being] in communication with a corresponding bond pad of said semiconductor device; and

at least one conductive trace in communication with said at least one electrically conductive via and carried on a surface of said substrate which is opposite from another surface of said substrate that is adjacent to said semiconductor device.